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Terms	Documents
L3 and (packet or data or information)	32

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<u>L4</u>	L3 same (packet or data or information)	1	<u>L4</u>
<u>L3</u>	L2 same (bus near5 interfac\$3)	32	<u>L3</u>
<u>L2</u>	L1 same (microengine or (micro adj1 engine))	64	<u>L2</u>
<u>L1</u>	((multi adj1 thread\$3) or multithread\$3) near5 processor	944	<u>L1</u>

END OF SEARCH HISTORY

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L6

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0 L6

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

32 L5

L5 L3 and (packet or data or information)

1 L4

L4 L3 same (packet or data or information)

32 L3

L3 L2 same (bus near5 interfac\$3)

64 L2

L2 L1 same (microengine or (micro adj1 engine))

944 L1

L1 ((multi adj1 thread\$3) or multithread\$3) near5 processor

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(370/910 370/912 370/412 370/444 709/230 709/200 709/245 709/220 710/39 710/52 710/100 710/260 710/310 710/5 710/300 710/34 711/154 711/100 711/101 712/244 712/225 712/10 712/220).ccls.	15073

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L7 710/39,52,100,260,310,5,300,34;709/230,200,245,220;711/154,100,101;712/244,225,10,220;370,

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L6 L5

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5 L3 and (packet or data or information)

L4 L3 same (packet or data or information)

L3 L2 same (bus near5 interfac\$3)

L2 L1 same (microengine or (micro adj1 engine))

L1 ((multi adj1 thread\$3) or multithread\$3) near5 processor

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 and L7	24

Database: US Pre-Grant Publication Full-Text Database
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L8 l2 and L7

L7 710/39,52,100,260,310,5,300,34;709/230,200,245,220;711/154,100,101;712/244,225,10,220,370.

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L6 L5

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5 L3 and (packet or data or information)

L4 L3 same (packet or data or information)

L3 L2 same (bus near5 interfac\$3)

L2 L1 same (microengine or (micro adj1 engine))

L1 ((multi adj1 thread\$3) or multithread\$3) near5 processor

END OF SEARCH HISTORY

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((multi adj1 thread\$3) or multithread\$3) same microengine
same control\$4

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6728845 B2	20040427	30	SRAM controller for parallel processor architecture and	711/154	710/39; 711/158
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6681300 B2	20040120	10	Read lock miss control and queue management	711/152	710/52; 711/104;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6671827 B2	20031230	8	Journaling for parallel hardware threads in	714/38	703/26
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6668317 B1	20031223	36	Microengine for parallel processor architecture	712/245	712/228
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6661794 B1	20031209	31	Method and apparatus for gigabit packet assignment	370/394	370/412
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6631462 B1	20031007	17	Memory shared between processing threads	712/225	711/132; 712/201;
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6631430 B1	20031007	12	Optimizations to receive packet status from fifo bus	710/100	710/52; 711/100
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6625654 B1	20030923	25	Thread signaling in multi-threaded network	709/230	709/200; 709/245;
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6611276 B1	20030826	26	Graphical user interface that displays operation of	345/772	345/771; 345/835;
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6606704 B1	20030812	35	Parallel multithreaded processor with plural	712/248	712/10; 712/228
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6587906 B2	20030701	10	Parallel multi-threaded processing	710/240	710/52; 718/104

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1 Threaded multiple path execution

Wallace, S.; Calder, B.; Tullsen, D.M.; Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on , 27 June-1 July 1998
Pages:238 - 249

[\[Abstract\]](#) [\[PDF Full-Text \(136 KB\)\]](#) **IEEE CNF**

2 Microprocessors for the new millennium: Challenges, opportunities, new frontiers

Gelsinger, P.P.; Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International , 5-7 Feb. 2001
Pages:22 - 25

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3 A workload generation environment for trace-driven simulation of shared-bus multiprocessors

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4 Proceedings of International Conference on Parallel Processing

Parallel Processing Symposium, 1996., Proceedings of IPPS '96, The 10th International , 15-19 April 1996

[\[Abstract\]](#) [\[PDF Full-Text \(480 KB\)\]](#) [IEEE CNF](#)

5 An architecture of on-chip-memory multi-threading processor

Matsuzaki, T.; Tomiyasu, H.; Amamiya, M.;

Innovative Architecture for Future Generation High-Performance Processors and Systems, 2001 , 18-19 Jan. 2001

Pages:100 - 108

[\[Abstract\]](#) [\[PDF Full-Text \(568 KB\)\]](#) [IEEE CNF](#)

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Threaded multiple path execution

Wallace, S. Calder, B. Tullsen, D.M.

Dept. of Comput. Sci. & Eng., California Univ., San Diego, La Jolla, CA, USA;
This paper appears in: Computer Architecture, 1998. Proceedings. The 2 Annual International Symposium on

Meeting Date: 06/27/1998 - 07/01/1998

Publication Date: 27 June-1 July 1998

Location: Barcelona Spain

On page(s): 238 - 249

Reference Cited: 13

Number of Pages: xiii+394

Inspec Accession Number: 5985663

Abstract:

This paper presents Threaded Multi-Path Execution (TME), which exploits existing hardware on a Simultaneous Multithreading (SMT) processor to speculatively execute multiple paths of execution. When there are fewer threads in an SMT processor than hardware contexts, threaded multi-path execution uses spare contexts to fetch code along the less likely path of hard-to-predict branches. This paper describes the hardware mechanisms needed to enable an SMT processor to efficiently speculatively execute multiple paths for threaded multi-path execution. The Mapping Scheduler is described which enables the spawning of these multiple paths. Policies are described for deciding which branches to fork, and for managing competition between parallel threads for critical resources. Our results show that TME increases the single program performance of an SMT with eight thread contexts by 14%-23% average, depending on the misprediction penalty, for programs with a high miss rate.

Index Terms:

parallel architectures performance evaluation synchronisation hard-to-predict branch synchronization bus simultaneous multithreading processor single program performance threaded multiple path execution

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An architecture of on-chip-memory multi-threading processor

Matsuzaki, T., Tomiyasu, H., Amamiya, M.

Dept. of Intelligent Syst., Kyushu Univ., Fukuoka , Japan;

This paper appears in: Innovative Architecture for Future Generation Hi Performance Processors and Systems, 2001

Meeting Date: 01/18/2001 - 01/19/2001

Publication Date: 18-19 Jan. 2001

Location: Maui, HI USA

On page(s): 100 - 108

Reference Cited: 10

Number of Pages: 109

Inspec Accession Number: 7106748

Abstract:

This paper proposes an on-chip-memory **processor** architecture: FUCE. FUCE Fusion of Communication and Execution. The goal of the FUCE **processor** pr fusing the intra **processor** execution and inter **processor** communication. In achieve this goal, the FUCE **processor** integrates the **processor** units, memo and communication units into a chip. FUCE **Processor** provides a next genera memory system architecture. In this architecture, no data cache memory is n since memory access latency can be hidden due to the simultaneous **multithi** mechanism and the on-chip-memory system with broad-bandwidth low latenc **bus** of FUCE **Processor**. This approach can reduce the performance gap betw instruction execution, and memory and network accesses

Index Terms:

[memory architecture](#) [multi-threading](#) [parallel architectures](#) [FUCE](#) [FUCE processor](#) [access latency](#) [memory system architecture](#) [multi-threading processor](#) [on-chip-mem](#) [processor architecture](#)

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US-PAT-NO: 6728845

Details view DOCUMENT-IDENTIFIER: US 6728845 B2

TITLE: SRAM controller for parallel processor architecture and method for controlling access to a RAM using read and read/write queues

----- KWIC -----

Detailed Description Text - DETX (3):

Referring to FIG. 1, a communication system 10 includes a parallel, hardware-based multithreaded processor 12. The hardware-based multithreaded processor 12 is coupled to a bus such as a peripheral component interface (PCI) bus 14, a memory system 16 and a second bus 18. The system 10 is especially useful for tasks that can be broken into parallel subtasks or functions. Specifically hardware-based multithreaded processor 12 is useful for tasks that are bandwidth oriented rather than latency oriented. The hardware-based multithreaded processor 12 has multiple microengines 22a-22f each with multiple hardware controlled threads that can be simultaneously active and independently work on a task.

Detailed Description Text - DETX (4):

The hardware-based multithreaded processor 12 also includes a central controller or core processor 20 that assists in loading microcode control for other resources of the hardware-based multithreaded processor 12 and performs other general purpose computer type functions such as handling protocols, exceptions, extra support for packet processing where the microengines pass the packets off for more detailed processing such as in boundary conditions. In one embodiment, the central controller or core processor 20 is a Strong Arm.RTM. (Arm is a trademark of ARM Limited, United Kingdom) based architecture. The general purpose microprocessor 20 has an operating system. Through the operating system the central controller or core processor 20 can call functions to operate on microengines 22a-22f. The central controller or core processor 20 can use any supported operating system preferably a real time operating system. For the central controller or core processor implemented as a Strong Arm architecture, operating systems such as, MicrosoftNT.RTM. (Microsoft Corporation, Redmond Wash.) real-time, VXWorks.RTM. (Wind River



US006728845B2

(12) United States Patent
Adiletta et al.(10) Patent No.: US 6,728,845 B2
(45) Date of Patent: *Apr. 27, 2004

(54) SRAM CONTROLLER FOR PARALLEL PROCESSOR ARCHITECTURE AND METHOD FOR CONTROLLING ACCESS TO A RAM USING READ AND READ/WRITE QUEUES

(75) Inventor: Matthew J. Adiletta, Worcester, MA (US); William Wheeler, Southborough, MA (US); James Redfield, Hudson, MA (US); Daniel Cutler, Townsend, MA (US); Gilbert Wolrich, Framingham, MA (US)

(73) Assignee: Intel Corporation, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: 10/208,264

(22) Filed: Jul. 30, 2002

(65) Prior Publication Data

US 2003/0145159 A1 Jul. 31, 2003

Related U.S. Application Data

(63) Continuation of application No. 09/387,110, filed on Aug. 31, 1999, now Pat. No. 6,427,196.

(31) Int. Cl. 7 G06F 13/00

(52) U.S. Cl. 711/134; 711/158; 710/39

(58) Field of Search 711/158, 151, 711/168, 169, 134; 710/39, 52, 54, 57, 112; 712/233

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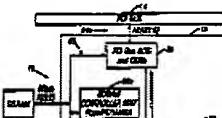
* cited by examiner

Primary Examiner—Glenn Gosage
(74) Attorney, Agent, or Firm—Fish & Richardson P.C.

(57) ABSTRACT

A controller for a random access memory (RAM), such as a static ram (SRAM), includes an address and command queue that holds memory references from a plurality of microcontroller functional units. The address and command queue includes a read queue that stores read memory references. The controller also includes a first read/write queue that holds memory references from a core processor and control logic including an arbiter that detects the fullness of each of the queues and a status of completion of outstanding memory references to select a memory reference from one of the queues. The memory controller may be used in parallel processing systems and may also include an order queue, a lock lookup content addressable memory (CAM) and a read lock fail queue. A system including a media access controller (MAC), a network processor and an SRAM controller, and a method for controlling a RAM, are also described.

18 Claims, 18 Drawing Sheets



US-PAT-NO: 6681300

DOCUMENT-IDENTIFIER: US 6681300 B2

TITLE: Read lock miss control and queue management

----- KWIC -----

Detailed Description Text - DETX (2):

Referring to FIG. 1, a communication system 10 includes a parallel, hardware-based multithreaded processor 12. The hardware-based multithreaded processor 12 is coupled to a bus such as a peripheral component interconnect (PCI) bus 14, a memory system 16, and a second bus 18. The system 10 is especially useful for tasks that can be broken into parallel subtasks or functions. Specifically, a hardware-based multithreaded processor 12 is useful for tasks that are bandwidth oriented rather than latency oriented. The hardware-based multithreaded processor 12 has multiple microengines 22a-22f, each with multiple hardware controlled threads that can be simultaneously active and independently work on a task.

Detailed Description Text - DETX (3):

The hardware-based multithreaded processor 12 also includes a central controller 20 that assists in loading microcode control for other resources of the hardware-based multithreaded processor 12 and performs other general purpose computer type functions such as handling protocols, exceptions, and extra support for packet processing where the microengines 22a-22f pass the packets off for more detailed processing such as in boundary conditions. In one embodiment, the processor 20 is a Strong Arm.RTM. (Arm is a trademark of ARM Limited, United Kingdom) based architecture. The general purpose microprocessor 20 has an operating system. Through the operating system the processor 20 can call functions to operate on microengines 22a-22f. The processor 20 can use any supported operating system, preferably a real time operating system. For the core processor implemented as a Strong Arm architecture, operating systems such as, MicrosoftNT real-time, VXWorks and .mu.CUS, a freeware operating system available over the Internet, can be used.

Detailed Description Text - DETX (7):

US-PAT-NO: 6668317

DOCUMENT-IDENTIFIER: US 6668317 B1

TITLE: Microengine for parallel processor architecture

----- KWIC -----

Abstract Text - ABTX (1):

A parallel hardware-based multithreaded processor is described. The processor includes a general purpose processor that coordinates system functions and a plurality of microengines that support multiple hardware threads. The processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references.

Detailed Description Text - DETX (3):

Referring to FIG. 1, a communication system 10 includes a parallel, hardware-based multithreaded processor 12. The hardware-based multithreaded processor 12 is coupled to a bus such as a peripheral component interface (PCI) bus 14, a memory system 16 and a second bus 18. The system 10 is especially useful for tasks that can be broken into parallel subtasks or functions. Specifically hardware-based multithreaded processor 12 is useful for tasks that are bandwidth oriented rather than latency oriented. The hardware-based multithreaded processor 12 has multiple microengines 22a-22f each with multiple hardware controlled threads that can be simultaneously active and independently work on a task.

Detailed Description Text - DETX (4):

The hardware-based multithreaded processor 12 also includes a central controller or core processor 20 that assists in loading microcode control for other resources of the hardware-based multithreaded processor 12 and performs other general purpose computer type functions such as handling protocols, exceptions, extra support for packet processing where the microengines pass the packets off for more detailed processing such as in boundary conditions. In



US06668317B1

(12) United States Patent
Bernstein et al.

(10) Patent No.: US 6,668,317 B1
(45) Date of Patent: Dec. 23, 2003

(54) MICROENGINE FOR PARALLEL PROCESSOR ARCHITECTURE

(75) Inventors: Dore Bernstein, Sudbury, MA (US); Donald F. Hooper, Sudbury, MA (US); Matthew J. Adelko, Worcester, MA (US); Gilbert Weisheit, Framingham, MA (US); William Wheeler, Southborough, MA (US)

(73) Assignee: Intel Corporation, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No. 09/387,046

(22) Filed: Aug. 31, 1999

(51) Int. Cl. 7 G06F 9/48

(52) U.S. Cl. 712/248, 712/228

(58) Field of Search 712/245, 228,

712/252, 40, 248; 705/213, 312

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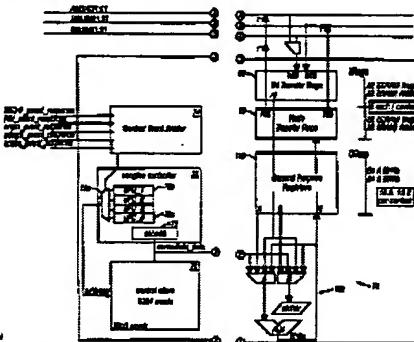
Primary Examiner—Eric Coleman

(74) Attorney, Agent, or Firm—Fish & Richardson P.C.

(57) ABSTRACT

A parallel hardware-based multithreaded processor is described. The processor includes a general purpose processor that coordinates system functions and a plurality of microengines that support multiple hardware threads. The processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references.

41 Claims, 23 Drawing Sheets



US-PAT-NO: 6427196

DOCUMENT-IDENTIFIER: US 6427196 B1

See image for Certificate of Correction

TITLE: SRAM controller for parallel processor architecture
including address and command queue and arbiter

----- KWIC -----

Detailed Description Text - DETX (3):

Referring to FIG. 1, a communication system 10 includes a parallel, hardware-based multithreaded processor 12. The hardware-based multithreaded processor 12 is coupled to a bus such as a peripheral component interface (PCI) bus 14, a memory system 16 and a second bus 18. The system 10 is especially useful for tasks that can be broken into parallel subtasks or functions. Specifically hardware-based multithreaded processor 12 is useful for tasks that are bandwidth oriented rather than latency oriented. The hardware-based multithreaded processor 12 has multiple microengines 22a-22f each with multiple hardware controlled threads that can be simultaneously active and independently work on a task.

Detailed Description Text - DETX (4):

The hardware-based multithreaded processor 12 also includes a central controller or core processor 20 that assists in loading microcode control for other resources of the hardware-based multithreaded processor 12 and performs other general purpose computer type functions such as handling protocols, exceptions, extra support for packet processing where the microengines pass the packets off for more detailed processing such as in boundary conditions. In one embodiment, the central controller or core processor 20 is a Strong Arm.RTM. (Arm is a trademark of ARM Limited, United Kingdom) based architecture. The general purpose microprocessor 20 has an operating system. Through the operating system the central controller or core processor 20 can call functions to operate on microengines 22a-22f. The central controller or core processor 20 can use any supported operating system preferably a real time operating system. For the central controller or core processor implemented as a Strong Arm architecture, operating systems such as, MicrosoftNT.RTM. (Microsoft Corporation, Redmond Washington) real-time, VXWorks.RTM. (Wind



US006427196B1

(12) United States Patent
Adleita et al.(10) Patent No.: US 6,427,196 B1
(45) Date of Patent: Jul 30, 2002

(54) SRAM CONTROLLER FOR PARALLEL PROCESSOR ARCHITECTURE INCLUDING ADDRESS AND COMMAND QUEUE AND ARBITER

(75) Inventor: Matthew J. Adleita, Worcester; William Whalen, Stowborough; James Radford, Hudson; Daniel Cuter, Townsend; Gilbert Wolrich, Birmingham, all of MA (US)

(73) Assignee: Intel Corporation, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/347,110

(22) Filed: Aug. 31, 1999

(51) Int. Cl. 7 G06F 13/08; G06F 9/00

(32) U.S. Cl. 711/158; 711/104; 710/39;

712/233

(58) Field of Search 711/104, 105,

711/151, 158, 168, 169; 710/39, 52, 54,

57, 112; 712/233

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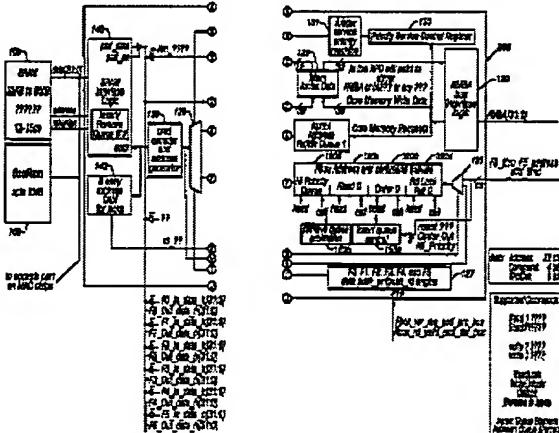
Primary Examiner—Glen Glassco

(74) Attorney, Agent, or Firm—Fish & Richardson P.C.

(57) ABSTRACT

A controller for a random access memory includes an address and command queue that holds memory references from a plurality of micro control functional units. The address and command queue includes a read queue that stores read memory references. The controller also includes a fine read/write queue that holds memory references from a core processor and control logic including an arbiter that detects the fullness of each of the queues and a status of completion of commanding memory references to select a memory reference from one of the queues.

17 Claims, 18 Drawing Sheets



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L4: Entry 1 of 1

File: PGPB

May 20, 2004

DOCUMENT-IDENTIFIER: US 20040095948 A1

TITLE: Data return arbitration

CLAIMS:

18. A network processor comprising: a plurality of multi-threaded packet processing microengines; a network interface; bus interfaces; memory interfaces; and a gasket linking the interfaces executing instructions in a command push pull bus format to a microarchitecture core executing instructions in a core memory bus format.

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L4: Entry 1 of 1

File: PGPB

May 20, 2004

PGPUB-DOCUMENT-NUMBER: 20040095948
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040095948 A1

TITLE: Data return arbitration

PUBLICATION-DATE: May 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lin, Chang-Ming	Cupertino	CA	US	

APPL-NO: 10/ 299948 [PALM]
DATE FILED: November 18, 2002

INT-CL: [07] H04 L 12/28, H04 L 12/56

US-CL-PUBLISHED: 370/412; 370/444
US-CL-CURRENT: 370/412; 370/444

REPRESENTATIVE-FIGURES: 3

ABSTRACT:

A system and method of arbitrating data return between simultaneous replies while maintaining priority over later replies is provided. The method includes receiving data in a plurality of priority buffers, detecting when two or more of the buffers are ready to read, storing unique identifications of the read-ready buffers in an order queue according to a priority of the buffer in which they are stored, and reading the unique identifications in the order queue in a first-in-first-out order.

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L9: Entry 1 of 1

File: USPT

Oct 7, 2003

US-PAT-NO: 6631430

DOCUMENT-IDENTIFIER: US 6631430 B1

TITLE: Optimizations to receive packet status from fifo bus

DATE-ISSUED: October 7, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wolrich; Gilbert	Fermingham	MA		
Bernstein; Debra	Sudbury	MA		
Adiletta; Matthew J.	Worc	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 473113 [PALM]

DATE FILED: December 28, 1999

INT-CL: [07] G06 F 12/00, G06 F 13/00

US-CL-ISSUED: 710/100, 710/52, 711/100

US-CL-CURRENT: 710/100; 710/52, 711/100

FIELD-OF-SEARCH: 710/107, 710/100, 710/22, 710/52, 711/100, 711/112, 711/213, 370/912, 340/286.01, 365/189.01

PRIOR-ART-DISCLOSED:

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<input type="checkbox"/> <u>6415338</u>	July 2002	Habot	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Fish & Richardson P.C.

ABSTRACT:

Receiving bytes of data from a media device includes issuing N consecutive requests, each for M-bytes, to the media device and receiving N-1 responses of M bytes of data from the media device.

30 Claims, 7 Drawing figures

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